## REMARKS

Claims 1-4, 6-20, 22-31 and 33-55 are pending. Claims 1, 10, 12, 17, 26, 28, 31, 40, and 42 have been amended, claims 5, 21, and 32 have been canceled, and new claims 45-55 have been added to recite additional features of Applicants' invention.

Reconsideration of the application is respectfully requested for the following reasons.

In the Office Action, claims 10, 12, 26, 28, 40, and 42 were rejected under 35 USC § 112, second paragraph, for failing to provide antecedent basis for various terms. Amendments have been presented to provide an antecedent basis for these terms. It is respectfully submitted that these amendments are sufficient to overcome the § 112, second paragraph, rejection.

Claims 1-8, 14-24, 30-38, and 44 were rejected under 35 U.S.C. § 1.102(e) for being anticipated by the Tsuda application. This rejection is respectfully traversed for the following reasons.

Claim 1 recites a noise suppression method comprising generating a frequency signal from a PLL based on a reference signal, and removing noise from the frequency signal by shifting a spurious signal of a predetermined order outside a loop bandwidth of the PLL. In addition to these features, claim 1 has been amended to recite "setting a frequency divider in a feedback loop of the PLL to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL." The Tsuda application does not disclose this setting step.

The Tsuda application discloses a technique for reducing noise in a phase-locked loop. As shown in Fig. 1, the PLL includes a loop circuit formed from a phase detector 1, a charge pump 2, a low pass filter 3, a voltage-controlled oscillator 4, and a feedback loop which includes a divider circuit 5. A control circuit 6 controls the feedback divider value, and a modulator circuit 7 modulates an input reference signal into the phase detector. In operation, a noise (or beat) component is shifted outside the pass band of the low pass filter in order to improve the signal-to-noise ratio of the PLL output. Unlike the claimed invention, however, modulator circuit 7 solely performs this shifting function:

> Modulator circuit 7 may shift the frequency of the beat component to a high frequency region which may be outside the pass band frequency of low pass filter (LPF) 3. In this way, the beat component may be prevented from being included in the low pass filter output LFPOUT used as a control signal for VCO4. (Emphasis Added)(See page 6, paragraph [0086]).

From the above, it is clear that the Tsuda technique is to use modulator circuit 7 to shift noise components outside the pass band of the low pass filter, where those components can then be removed. Claim 1, however, recites that a frequency divider in the feedback loop of the PLL shifts a spurious signal of a predetermined order outside the loop bandwidth of the PLL. The Tsuda application does not disclose or suggest these features, i.e., the Tsuda application discloses that reference signal modulator 7 performs a noise-shifting function not a divider circuit in the PLL feedback loop (e.g., divider 5).

Because the Tsuda application does not disclose all of the features recited in claim 1, it is respectfully submitted that claim 1 can not be anticipated by this reference. It is further submitted that the foregoing differences are sufficient to render claim 1 and its dependent claims non-obvious and thus patentable over the Tsuda application.

Incidentally, it is noted that the Tsuda application discloses controlling divider 5 by a signal-delta modulator for removing spurious pattern noise. However, this type of noise is not noise generated within the loop bandwidth of the PLL (e.g., within the pass band of the low pass filter 3). Rather, the Tsuda application discloses that reference modulator 7 is used to remove noise of this type.

Claim 17 recites a frequency generator comprising a noise suppressor which shifts a spurious signal of a predetermined order outside a loop bandwidth of a phased locked loop. In addition to these features, claim 17 has been amended to recite that the noise suppressor includes: a frequency divider and a feedback loop of a phase-locked loop, and "a controller which sets the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the phase-locked loop." As noted in the previous discussion, the Tsuda application does not disclose a controller of this type. Accordingly, it is submitted that claim 17 and its dependent claims are patentably distinguishable from the Tsuda application.

Claim 31 recites a frequency generator comprising a modulator which modulates a reference signal and a PLL which generates a frequency signal based on the modulator reference signal. The modulator generates a frequency separation between harmonics of the modulated reference and a reference signal that suppresses noise in the frequency signal. In addition to these features, claim 31 has been amended to recite that the PLL generates the frequency signal using the modulated reference signal "as long as the harmonics of the modulated reference signal are not coincident with the harmonics of the reference signal." The Tsuda application does not disclose or suggest these features. In reviewing the Office Action, it has appeared that the Examiner overlooked these features of the invention as no specific comments were directed to the reason why claims 31 and 32 were rejected. Applicants submit that claim 31 as amended is allowable.

Claim 33 recites a system for controlling the PLL. The system includes a divider which divides a frequency signal output from the PLL, and "a controller which sets the divider to a value which shifts a spurious noise signal of a predetermined order outside the loop bandwidth of the PLL." As previously discussed, the Tsuda application does not disclose a controller of this type. Accordingly, it is submitted that claim 33 and its dependent claims are patentably distinguishable from the Tsuda application.

New claims 45-55 have been added to the application.

Claim 45 recites that the spurious signal of claim 1 is "generated from a mismatch in at least one of the charge pump and a phase/frequency detector in the PLL." (See, for example, pages 2, 7, and 8 of the specification for support.) The Tsuda application does not disclose these features. In paragraph [0086], Tsuda discloses that modulator circuit 7 shifts a noise signal outside the pass band frequency of low pass filter 3. This noise signal is described as a beat component derived from an output signal sneaking into an input side of the phase comparison circuit 1 of the PLL. This type of noise is more precisely described in paragraph [0018] as emanating from the chip package, a power supply line, or a ground line. None of these types of noise correspond or otherwise result from a mismatch in at least one of the charge pump and a phase/frequency detector in the PLL, as recited in claim 45. Based on at least these differences, it is respectfully submitted that claim 45 is allowable over the Tsuda application. Claims 14, 30, and 44 recite features similar to claim 45 and therefore are also allowable.

Claim 46 recites that the mismatch in the charge pump includes "a mismatch between UP and DOWN current sources." The Tsuda application does not disclose these features.

Claim 47 recites that the mismatch in the phase/frequency detector includes "a mismatch between UP and DOWN signal paths in the phase/frequency detector." The Tsuda application does not disclose these features.

Claim 48 recites that the value of the frequency divider is set based on a modulation ratio of a signal-delta modulator for removing the spurious signal. The Tsuda application does not disclose these features. As previously discussed, the reference modulator 7 of the Tsuda circuit performs the shifting required for noise suppression. The Tsuda application does not disclose that divider 5 or control circuit 6 performs the shifting function required to suppress the type of spurious signal recited in claim 1. Absent a disclosure of these features, it respectfully submitted that the Tsuda application cannot anticipate nor render obvious claim 48.

Claim 49 recites that the frequency divider is a pulse swallow frequency divider which includes "a swallow counter and a program counter" and that "values for at least one of the swallow and program counters are controlled based on the modulation ratio of the signal-delta modulator." The Tsuda application does not disclose these features.

Claim 50 recites that a numerator of the modulation ratio is at least 50% of a denominator of the modulation ratio. (See, for example, Table 1 in the specification for support.) The Tsuda application does not disclose these features.

Claim 51 recites modulating the reference signal into the PLL with the reference modulator and that the reference modulator has a modulation ratio $IN_{MOD}$ is at least 50% of $D_{MOD}$. (See, for example, Table 1 in the specification for support.) The Tsuda application does not disclose these features.

Claim 52 recites adjusting at least one of a swallow counter and a program counter in the frequency divider to a value which shifts the spurious signal of said predetermined order outside the loop bandwidth of the PLL. The Tsuda application does not disclose these features.

Claim 53 recites "shifting the reference signal to a fractional fixed value for input into a phase/frequency detector of the PLL, said fractional fixed value further shifing the spurious signal of said predetermined order." The Tsuda application discloses a frequency modulator for modulating an input reference signal, but this modulator does not shift the input reference signal to a fractional fixed value that produces the shifting recited in claim 53. It is submitted that claim 53 is allowable for at least these reasons, along with claims 54 and 55 which recite similar subject matter depending from claims 17 and 31 respectively.

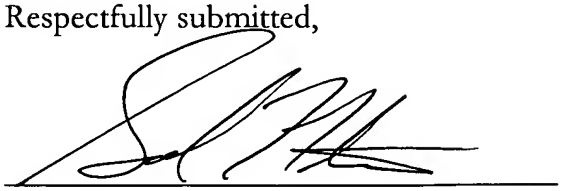
Reconsideration and withdrawal of all the rejections and objections made by the Examiner is hereby respectfully requested.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and prompt allowance of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with this application, including

extension of time fees, to Deposit Account No. 16-0607 (Attorney Docket No. GCTS-29) and credit any excess fees to the same Deposit Account.

Respectfully submitted,



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